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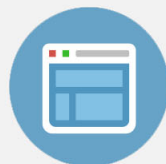
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Influence of interlayer trapping and detrapping mechanisms on the electrical characterization of hafnium oxide/silicon nitride stacks on silicon

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Al/HfO₂/SiN_x:H/*n*-Si metal-insulator-semiconductor capacitors have been studied by electrical characterization. Films of silicon nitride were directly grown on *n*-type silicon substrates by electron cyclotron resonance assisted chemical vapor deposition. Silicon nitride thickness was varied from 3 to 6.6 nm. Afterwards, 12 nm thick hafnium oxide films were deposited by the high-pressure sputtering approach. Interface quality was determined by using current-voltage, capacitance-voltage, deep-level transient spectroscopy (DLTS), conductance transients, and flatband voltage transient techniques. Leakage currents followed the Poole-Frenkel emission model in all cases. According to the simultaneous measurement of the high and low frequency capacitance voltage curves, the interface trap density obtained for all the samples is in the 10¹¹ cm⁻² eV⁻¹ range. However, a significant increase in this density of about two orders of magnitude was obtained by DLTS for the thinnest silicon nitride interfacial layers. In this work we probe that this increase is an artifact that must be attributed to traps existing at the HfO₂/SiN_x:H intralayer interface. These traps are more easily charged or discharged as this interface comes near to the substrate, that is, as thinner the SiN_x:H interface layer is. The trapping/detrapping mechanism increases the capacitance transient and, in consequence, the DLTS measurements have contributions not only from the insulator/substrate interface but also from the HfO₂/SiN_x:H intralayer interface.

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I. INTRODUCTION

High permittivity (high-*k*) dielectrics are nowadays being subject of great study in order to replace SiO₂ as gate dielectric in metal-oxide-semiconductor field-effect transistors in the future scales of integration.^{1,2} To achieve performance comparable to silicon oxide, high-*k* dielectrics have to fulfill some requirements: high quality interface with Si, thermodynamic stability in contact with Si, high recrystallization temperature, high bandgap, and lower leakage conduction than silicon oxide at an equivalent oxide thickness. HfO₂-based materials are among the most promising of such materials.¹⁻³

However, before these materials can replace SiO₂ as gate dielectric, the nature and formation of electrically active defects existing in these emerging materials should be known. These defects play an important role in device operation: They can cause channel mobility degradation, bias instability,⁴ and leakage current increase.⁵ Defects in SiO₂ are passivated by hydrogen, but this can cause some problems in HfO₂.⁶ Moreover, as most of the high-*k* materials, when deposited in direct contact with Si an interfacial layer (few nanometers thick) is formed.⁷ We have confirmed, in an earlier work, the formation of silicon oxide (SiO_x) as interfacial layer when depositing HfO₂ on Si.⁸ This noncontrolled

interfacial layer can increase interfacial state density *D*_{it} and leakage current. A general practice has been to grow a controlled free-defect SiO₂ barrier layer between substrate and high-*k* dielectric, thick enough to avoid reaction. Unfortunately, this barrier layer leads to a reduction of the dielectric constant and, hence, to the effective capacitance of the gate dielectric stack, impeding to reach the necessary equivalent oxide thickness (EOT) values. The use of silicon nitride instead of silicon oxide as a barrier layer can improve the effective capacitance of the gate dielectric stack, since silicon nitride has a higher permittivity (*k*_{Si₃N₄} ~ 7) than silicon oxide (*k*_{SiO₂} ~ 3.9). Moreover, SiN_x layer prevents the growth of silicon oxides when high-*k* dielectric is deposited and it is known that the use of nitrides greatly reduces boron diffusion from the heavily doped poly-Si gate electrode to the lightly doped Si channel.⁹

This work presents an electrical study of Al/HfO₂/SiN_x:H/*n*-Si metal-insulator-semiconductor (MIS) structures. Hafnium oxide was grown by high-pressure sputtering (HPS) (Ref. 10) using Ar as processing gas, while silicon nitride was grown by electron cyclotron resonance-chemical vapor deposition (ECR-CVD), using SiH₄ and N₂ as precursors. We have studied the effect of SiN_x:H thickness in the electrical characteristics while keeping HfO₂ thickness constant at 12 nm. Besides silicon nitride thickness effect, another important subject to study is the thermal annealing effects on the characteristics of dielectric films, since high-temperature anneals are generally used in chip technol-

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TABLE I. ECR-CVD time and silicon nitride thickness of samples deposited for electrical characterization.

Sample	ECR-CVD time (s)	Silicon nitride thickness (nm)	RTA
Asd_1	90	6.6 ± 0.4	As deposited
RTA_1			600 °C–30 s
Asd_2	60	5.9 ± 0.4	As deposited
RTA_2			600 °C–30 s
Asd_3	30	3.9 ± 0.2	As deposited
RTA_3			600 °C–30 s
Asd_4	15	3.0 ± 0.4	As deposited
RTA_4			600 °C–30 s

ogy for dopant activation. Because of that, we have also compared the electrical properties of as-deposited films with those corresponding to samples submitted to rapid thermal annealing (RTA). Techniques used to study MIS structures were current-voltage (I - V), 1 MHz capacitance-voltage (C - V), deep-level transient spectroscopy (DLTS), simultaneous high and low frequency capacitance-voltage (HLCV), conductance transients (G - t), and constant-capacitance flat-band voltage transients (V_{FB} - t).

II. EXPERIMENTAL

MIS structures were obtained as follows: Substrates used were n -Si (polished on one side, 5 Ω cm resistivity, and 500 μ m thick). Before the dielectric films were deposited on the substrates, these were submitted to a standard Radio Corporation of America cleaning.¹¹ Deposition of silicon nitride was conducted in a homemade chamber attached to an ECR Astex 4500 reactor. A mixture of high purity silane (SiH_4) and N_2 was used as precursors. Deposition times were 90, 60, 30, and 15 s giving rise to four different thicknesses (6.6, 5.8, 3.9, and 3 nm, respectively). Two series were obtained for each thickness, being one of them submitted to a RTA in argon at 600 °C for 30 s. Afterwards, 12 nm HfO_2 films were grown in a HPS system at pressure of 1.2 mbars during 30 min, keeping the temperature at 200 °C. High- k dielectric films were grown in a pure Ar atmosphere, because a preliminary study showed that these films presented an amorphous structure.¹² After the dielectric deposition, aluminum dot electrodes were e-beam evaporated through a shadow mask. Table I lists the samples obtained for electrical measurements.

The structures were characterized by means of Fourier transformed infrared (FTIR) spectroscopy using a Nicolet Magna-IR 750 series II spectrometer working in transmission mode at normal incidence, and by cross section transmission electron microscopy (TEM) with a JEOL-JEM-2000FX microscope operating at 200 keV.

Electrical measurements were carried out putting the sample in a light-tight, electrically shielded box. In order to record electrical parameters at temperatures varying between room temperature and 77 K, samples were cooled in an Oxford DM1710 cryostat. An Oxford ITC 503 controller was used to keep the temperature constant during isothermal measurements such as DLTS, flatband voltage transients, and

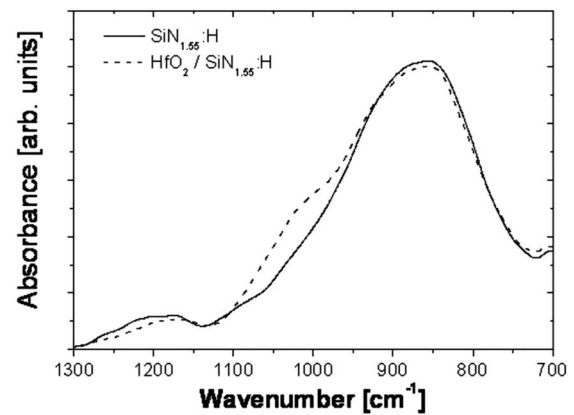


FIG. 1. FTIR spectrum of a $\text{HfO}_2/\text{SiN}_{1.55}/\text{H}/\text{Si}$ stack (dotted line). Also shown, the FTIR spectra of a $\text{SiN}_{1.55}/\text{H}$ film (solid line). Notice that the peak position of the main $\text{SiN}_{1-x}/\text{H}$ vibration is unaffected after the HfO_2 plasma deposition process.

conductance transients. C - V measurement setup involved a 1 MHz Boonton 72B capacitance meter and a Keithley 617 programmable electrometer. The experimental setup of the conductance transient technique consists of an HP 33120A arbitrary wave form generator to apply the bias pulses, an EG&G 5206 two phase lock-in analyzer to measure the conductance, and an HP 54501A digitizing oscilloscope to record the complete conductance transients. An Agilent N6700B bias source, a Keithley 6517A electrometer, and a Boonton 72B capacitance meter were used for recording flat-band voltage transients at constant capacitance.

To determine the interface trap density we used DLTS and HLCV in order to contrast the results obtained by these two different techniques. DLTS measurements were carried out using the Boonton 72B capacitance meter, an HP 54501 digital oscilloscope to record the capacitance transients, and an HP 81104A pulse generator to bias the samples from inversion to accumulation. The simultaneous measurement of the HLCV curves was carried out by means of a Keithley Model 82 system.

Finally, the I - V curves were measured biasing the samples with an Agilent N6700B and measuring the current with a Keithley 6517A programmable electrometer.

III. RESULTS AND DISCUSSION

A. Structure and composition of the films

The FTIR spectra of the SiN_x/H thin film, and the $\text{HfO}_2/\text{SiN}_x/\text{H}$ stacked structure obtained after HfO_2 deposition in Ar atmosphere are shown in Fig. 1. The FTIR spectrum of the SiN_x/H layer has the characteristic Si–N stretching band located at 844 cm^{-1} .¹³ After the HfO_2 deposition, a smooth shoulderlike feature appears at about 1018 cm^{-1} , slightly above the frequency corresponding to the Si–O–Hf configuration (970 cm^{-1}).¹⁴ We tentatively attribute this band to the vibration of bonding groups involving Si, O, N, and Hf, which may be formed at the HfO_2/SiN interface in small concentration.

In Fig. 2, a TEM image of a typical structure in which SiN_x/H film has a 2.9 nm thickness is shown. From the figure, a smooth surface topography can be observed. Also

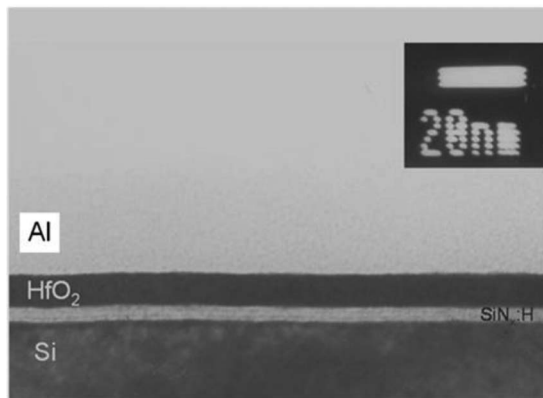


FIG. 2. Cross sectional image of a $\text{HfO}_2/\text{SiN}_x\text{:H}$ structure. $\text{SiN}_x\text{:H}$ thickness is 2.9 nm.

well defined $\text{SiN}_x\text{:H}/\text{Si}$ and $\text{HfO}_2/\text{SiN}_x\text{:H}$ interfaces can be clearly seen. The TEM image shows that the $\text{SiN}_x\text{:H}$ film is unaltered after the deposition of the amorphous HfO_2 film in Ar plasma.

B. Electrical measurements

Figure 3 shows 1 MHz C - V curves measured at room temperature for as-deposited samples [Fig. 1(a)] and for annealed samples [Fig. 1(b)]. Theoretical flatband voltage for $\text{Al}/\text{HfO}_2/\text{SiN}_x\text{:H}/n\text{-Si}$ structures is about -0.3 eV.¹⁵ The thinnest sample exhibits flatband voltages close to the theoretical value, but as silicon nitride layer thickness increases, flatband voltage shifts toward more negative values, so positive charge is accumulating in the dielectric film. This positive charge can be due to hydrogen that comes from silane precursor: As SiN_x thickness increases, more hydrogen can be accumulated in the film increasing the voltage shift.

Samples corresponding to the two thickest dielectric films show clockwise hysteresis (both as deposited and annealed). This fact indicates that there are slow states in dielectric films, i.e., defects distributed away from the interface to the insulator, called disordered induced gap states (DIGS).¹⁶ We can obtain a three-dimensional plot of DIGS density as a function of energy position and spatial position by measuring conductance transients (G - t).^{17,18} DIGS density values are listed in Table II, which also shows other electrical characterization results. Conductance transients have only been observed in films that show hysteresis phenomena. DIGS density is higher in 5.84 nm thick samples than in 6.64 nm thick ones (both in as-deposited and in annealed samples). However, no conductance transients were observed in the thinnest samples. Figure 4 shows the contour plot of DIGS, corresponding to Asd_2 sample, as a function of distance to substrate interface (X_c) and of energetic position, being $E_T - E_{Csc}$ the energy position of the traps with respect to the silicon band edge. The energetic position of DIGS is similar in all measured samples. When recording a conductance transient, capture processes take place in which the empty DIGS trap electrons (n -Si substrate here) coming by tunneling from the semiconductor conduction band. States near the insulator/semiconductor interface capture carriers before those located deeper in the dielectric. DIGS lo-

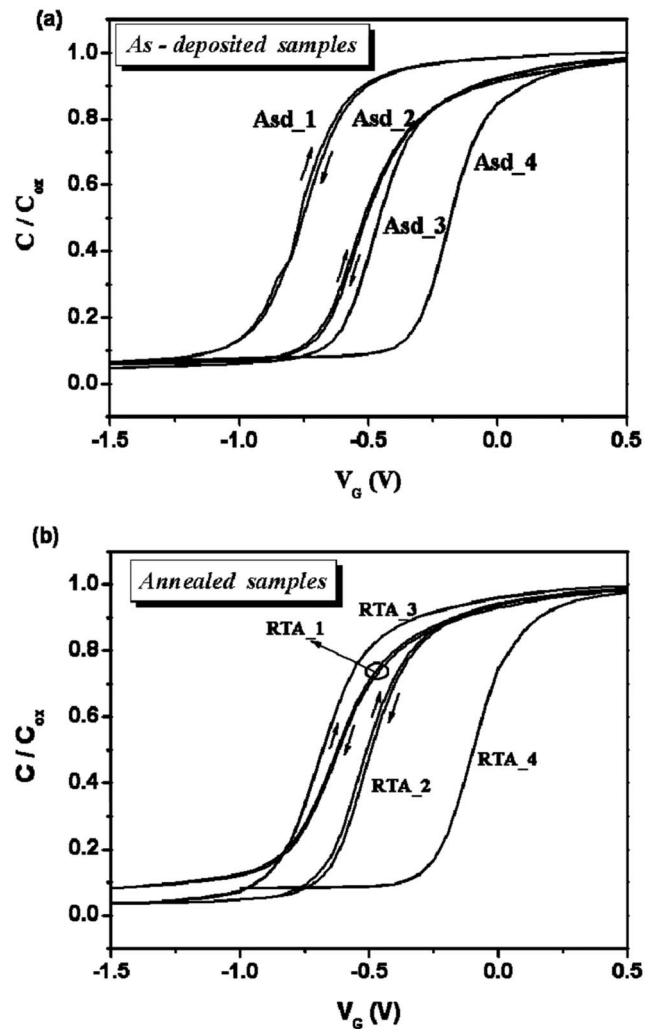


FIG. 3. 1 MHz C - V curves measured at room temperature corresponding to as-deposited samples (a) and to RTA samples (b).

ated very close to $\text{SiN}_x\text{:H}/n\text{-Si}$ interface have capture times much lower than our experimental constant time and cannot be recorded. That is the reason why the contour plots show DIGS densities for states located at distances higher than 1.7 nm from the interface. In Fig. 4 we also observe that the DIGS distribution has a maximum at a depth of about 1.9–2.0 nm, which is close to the $\text{SiN}_x\text{:H}$ thickness in the two thinnest samples. For these samples, we suggest that this region is very influenced by the presence of the interface with the HfO_2 layer and the states existing at this interface are predominant and, in consequence, no slow-trap related conductance transients are recorded. DIGS density increases when samples are submitted to a rapid thermal annealing suggesting that annealing creates more traps in the silicon nitride bulk.

We have also measured flatband voltage transients ($V_{FB} - t$). These transients are recorded by keeping constant the capacitance at flatband condition. Flatband transients are related to the hysteresis behavior, as conductance transients. In fact, these transients give information about phonon-assisted tunneling mechanisms between localized states in the band-gap of the insulator.¹⁹ As expected, transient amplitude is bigger in samples, which show hysteresis phenomena. In

TABLE II. Electrical characterization results of Al/HfO₂/SiN_x:H/*n*-Si MIS structures. DIGS is the maximum density of disorder induced gap states. Flatband voltage transients have been measured at room temperature (295 K). D_{it} is the interface state density measured by DLTS and simultaneous measurement of *C-V* curves at high and low frequency. activation energy values and PF coefficients are obtained from current measurements.

Sample	$N_{DIGS} \times 10^{10}$ (cm ⁻² eV ⁻¹)	Flatband voltage transients (mV)	D_{it} from DLTS $\times 10^{11}$ (cm ⁻² eV ⁻¹)	D_{it} from HLCV $\times 10^{11}$ (cm ⁻² eV ⁻¹)	Activation energy ΔE_{σ} (meV)	PF coefficient $\beta_{PF} (\times 10^{11})$ (eV m ^{1/2} V ^{-1/2})	k optical frequencies
Asd_1	1.9	5 mV	3–5	3.0		Not measured	
RTA_1	3.3	14 mV	2–5	2.2		Not measured	
Asd_2	8.0	10 mV	0.8–1	1.3	90.80	4.6	2.75
RTA_2	13.5	20 mV	1–2	2.7	84.3	11.1	0.47
Asd_3	Not detected	4 mV	Not measured	4.5	79.7	4.4	2.94
RTA_3	Not detected	4 mV	100–200	4.4	77.4	11.0	0.48
Asd_4	Not detected	Not detected	50–100	2.0	72.7	11.6	0.43
RTA_4	Not detected	Not detected	50–100	1.9	71.2	12.5	0.37

Table II, we can see the amplitude values of these transients. Measurements have been carried out at room temperature (295 K), biasing the samples in inversion regime (negative bias) as initial condition before starting the measurement. Figure 5 shows normalized flatband voltage transients corresponding to the two thickest samples (both as deposited and rapid thermal annealed). In all cases, we can see ascending transients (flatband voltage increasing with time), in good agreement with the clockwise hysteresis observed in *C-V* curves and the initial bias (inversion). Annealed samples show bigger flatband transients than as-deposited ones, in agreement with *G-t* measurements: As it has been said before, when samples are submitted to RTA, conductance transient amplitude increases, so DIGS density also increases.

Interface state densities (D_{it}) measured by DLTS are shown in Fig. 6. These results have been divided into two different groups: the one corresponding to the two thickest samples shows the lowest D_{it} density (from 8×10^{10} to 4×10^{11} cm⁻² eV⁻¹), and the other corresponding to the two thinnest samples exhibits the highest D_{it} density (from 6×10^{12} to 2×10^{13} cm⁻² eV⁻¹). The interface trap density was also determined by means of the simultaneous measurement of the HLCV curves. The values obtained are shown in Table II and are in the 10^{11} eV⁻¹ cm⁻² range for all the samples. It is clear that there are noticeable differences between these two techniques. We attribute these discrepancies so that the traps existing at HfO₂/SiN_x:H interface can

charge or discharge more easily as this interface comes near the substrate. When considering the particular values of bandgap, and conduction and valence band offsets of HfO₂ and Si₃N₄,²⁰ the energy band diagrams of the HfO₂/Si₃N₄/*n*-Si system under accumulation and inversion regimes are like those shown in Fig. 7. In this figure we observe that, at inversion, two-dimensional energy wells appear both for electrons (*e*-well) and holes (*h*-well) at the HfO₂/Si₃N₄ interface. This band energy structure remembers the typical one for a floating gate memory, being HfO₂ the blocking oxide (for holes), silicon nitride the tunneling film, and the interface between them would act as a two-dimensional charge trapping layer. Therefore, some charge can be trapped in the wells that screen the charge at the insulator-gate/semiconductor interface (Q_{it}). Depending on the balance between positive and negative charge amounts trapped at these wells, the charge at the metal electrode will be higher or lower than that induced by Q_{it} . When the positive charge at the *h*-well is higher than the negative one at the *e*-well, the total (negative) charge at the gate electrode, Q_G , is higher than the corresponding for only Q_{it} . On the contrary, when negative charge at the *e*-well prevails, Q_G is lowered. According to the energy band diagram of Fig. 7, charges at the *e*-well consist of electrons coming by tunneling from the gate electrode, whereas the *h*-well consists of

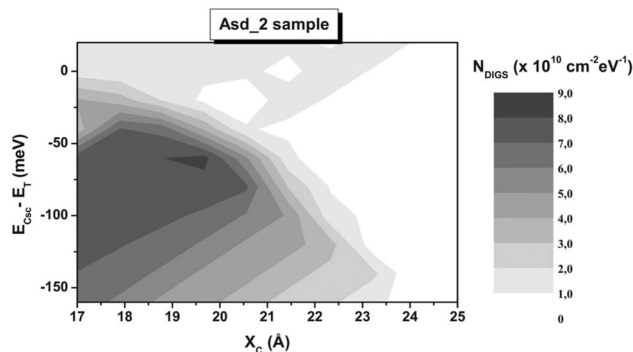


FIG. 4. Contour plot of DIGS density obtained from Asd_2 sample. X_C means the spatial distance to the dielectric/silicon substrate interface, and $E_T - E_{Csc}$ is the energy position of the traps with respect to the silicon band edge.

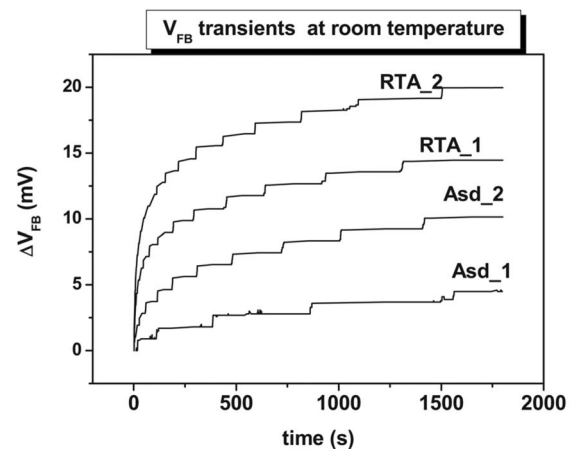


FIG. 5. Normalized flatband voltage transients measured at room temperature (295 K). Samples initially biased in inversion regime.

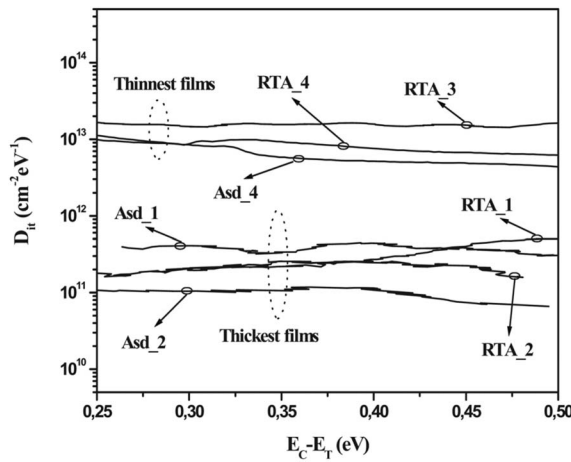


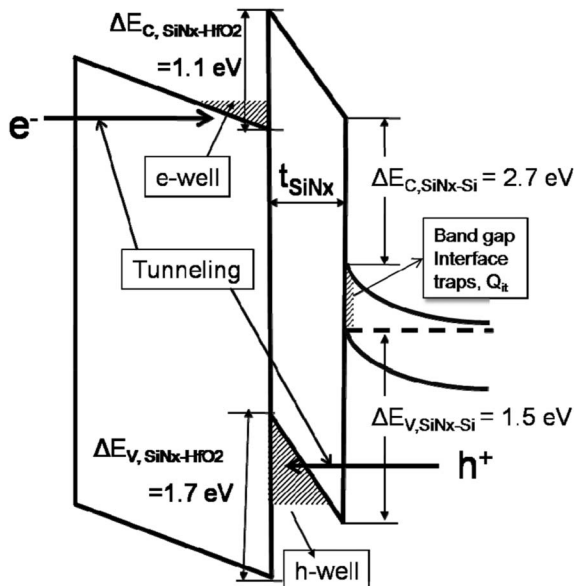
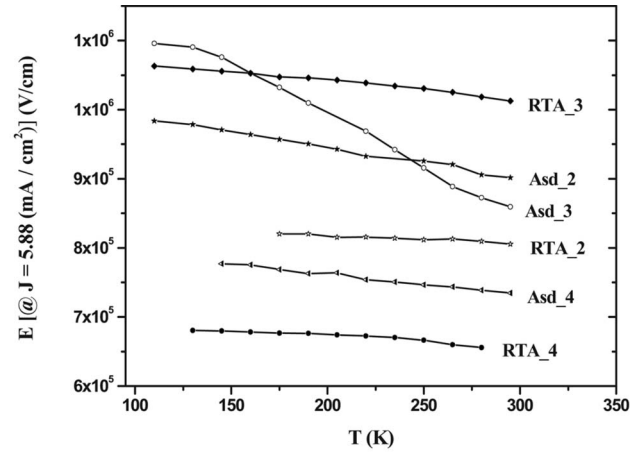
FIG. 6. Interfacial state density measured by DLTS.

holes coming from the semiconductor substrate also by tunneling. Since tunneling probability depends on the corresponding barrier thickness, we can conclude that as thinner the Si_3N_4 or as thicker the HfO_2 layers as more negative the value of Q_G .

In our experiment we kept constant the HfO_2 thickness, so the e -well trapped charge is the same for all the samples. On the contrary, the Si_3N_4 layer thickness has been varied from around 3 to 6.6 nm. To estimate the relationship between the tunneling charging/discharging probabilities between the h -well and the silicon substrate for two samples with different Si_3N_4 thicknesses (t_1 and t_2), we can use the following quantum mechanics expression:

$$\frac{p_1}{p_2} = \exp \left[\frac{2\pi\sqrt{2m_h\varphi_v}}{h} (t_1 - t_2) \right], \quad (1)$$

where m_h is the hole effective mass inside the barrier, φ_v is the mean barrier height, t_1 and t_2 are the barrier thicknesses, and h is Planck's constant. For the h -well triangular barrier

FIG. 7. Energy band diagram of the $\text{HfO}_2/\text{SiN}_x\text{:H}/\text{Si}$ MIS structure at inversion.FIG. 8. Average electric field values corresponding to 5.88 mA cm^{-2} current density as a function of temperature.

$\varphi_v = \Delta E_V/2$, where ΔE_V is the valence band offset of silicon nitride relative to silicon. Gritsenko and Meerson²¹ reported values of $\Delta E_V \approx 1.5 \text{ eV}$ and $m_h/m_0 = (0.3 \pm 0.1)$. Here m_0 is the free electron mass. These values yield a relation of $p_1/p_2 = 10^{-4}$ for two layers of 6 and 3 nm, respectively, so indicating that the “memory effect” of the thicker layer is negligible for thicker samples. However, that is not the case for the thinnest ones, increasing the total charge variation at the gate electrode. In summary, we can conclude that interface state densities obtained by DLTS in the specific case of the $\text{HfO}_2/\text{SiN}_x\text{:H}/\text{Si}$ system provide overestimated D_{it} values for very thin silicon nitride layers. A detailed revision of the DLTS formulation must be done for this case, which lies outside the scope of this paper.

From the results obtained by the HLCV method we observe that RTA slightly increases D_{it} density in the samples. No crystallization of silicon nitride is expected at this annealing temperature (600°C)^{22,23} and even in $\text{Al}/\text{SiN}_x\text{:H}/\text{Si}$ structures, interface state density decreases when a RTA is applied to the samples.²⁴ Anyway, these values are lower than those we obtained in an earlier work⁸ where we used a SiO_2 barrier layer instead of $\text{SiN}_x\text{:H}$. In that case we obtained D_{it} values of about $3 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ slightly higher than that obtained here for silicon nitride layers thick enough.

Figure 8 shows the electric field values corresponding to 5.88 mA/cm^2 current density, at temperatures between 77 and 295 K. Leakage current has only been measured under accumulation condition (positive bias) because the current saturates in inversion due to limited supply of minority carriers from the substrate.²⁵ The electric field used in this figure is an average value in the insulator stack. Since two different materials are present in the stack, the electric field is not constant in the entire insulator. We define this average field as

$$E = \frac{(V_G - V_{FB} - \Psi_s)}{t_{\text{HfO}_2} + t_{\text{SiN}_x\text{:H}}} \quad (2)$$

As current density is measured in accumulation, surface potential Ψ_s is negligible. There is a clear relation between C-V curves and conduction behavior: Samples that show low flat-

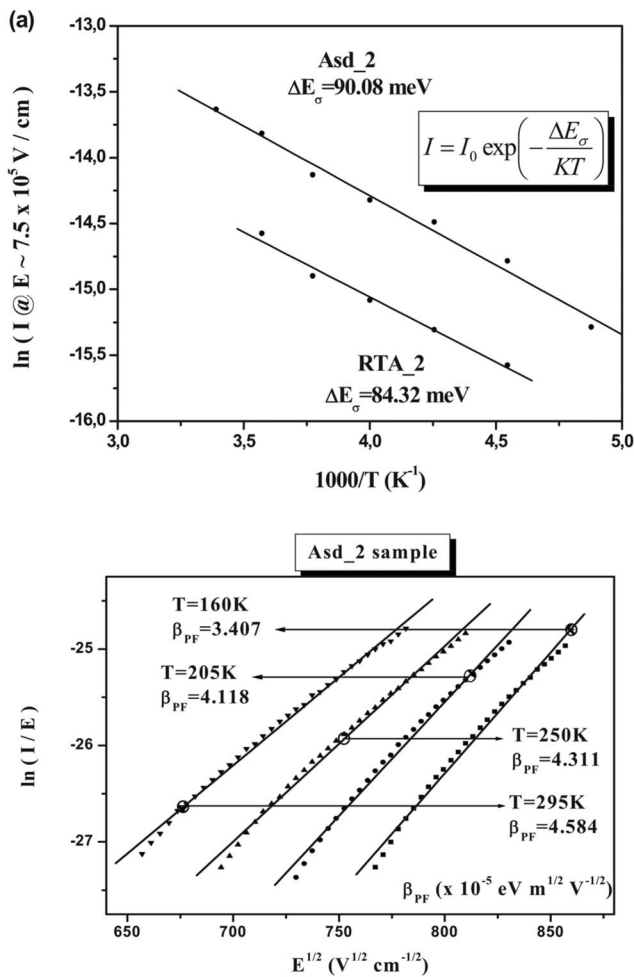


FIG. 9. Temperature dependence of the current measured at about 7.5×10^5 V/cm corresponding to Asd_2 and RTA_2 samples (a). Current-electric field dependence at several temperatures for Asd_2 sample (b).

band voltage shifts provide higher currents. Leakage current should be limited by HfO_2 , since at positive bias the conduction is controlled by the metal-oxide interface.²⁶ Hafnium oxide thickness is the same for all the films (12 nm), but the thinnest dielectric films show the highest leakage current. However, as silicon nitride layer thickness decreases the real electric field in hafnium oxide increases and becomes higher than the effective electric field, so the real differences in the samples should be less than the ones displayed. These results are also an improvement with respect to the case in which the silicon nitride barrier layer was not used.⁸ In that case the current densities were higher: Electric field value was 0.55 MV cm^{-1} for a 2.5 mA/cm^2 current density in a sample in which an 11 nm thick HfO_2 was directly deposited on $n\text{-Si}$.⁸ Moreover, in this last sample, a noncontrolled 3.63 nm thick SiO_x film was formed during high- k dielectric growth and the EOT was higher than for all the samples grown here. The lower leakage currents and the higher EOT values prove the utility of the silicon nitride barrier layer.

Figure 9(a) shows the current-temperature dependence for the samples Asd_2 and RTA_2. The relationship between $\ln(I)$ and $1000/T$ is clearly linear in the range 200–300 K. This linear behavior indicates a conduction mechanism controlled by the Poole–Frenkel (PF) model. The PF mechanism

is bulk limited, depends on insulator traps, and is associated with the field-enhanced thermal excitation of charge carriers from traps. If the slope of the lines does not vary with the applied field, this indicates that the conduction takes place through an activated process having single activation energy, ΔE_σ , following the relation²⁷

$$I = I_0 \exp\left(-\frac{\Delta E_\sigma}{KT}\right). \quad (3)$$

The activation energy values corresponding to all the measured samples are listed in Table II. Values obtained are similar in all the samples, but as silicon nitride thickness increases, activation energy values slightly increase (from 71.19 to 90.80 meV) and these values move away from the value earlier obtained in $\text{Al}/\text{HfO}_2/n\text{-Si}$ structure (50 meV).⁸

It is known that the relationship between the current and the electric field in PF conduction mechanism is²⁸

$$I = CE \exp\left(\frac{\beta_{\text{PF}} \sqrt{E} - q\phi_T}{KT}\right), \quad (4)$$

where C is a constant related to the density of ionized traps and carrier mobility, β_{PF} is the barrier lowering coefficient for PF emission, and ϕ_T is the ionization energy of the trap level. Figure 9(b) shows the plot of I/E (in logarithmic scale) against $E^{1/2}$ at several temperatures for the Asd_2 sample. The dependence is clearly linear, as required by the PF mechanism. The obtained values of the barrier lowering coefficient, β_{PF} , are similar for all the temperatures. The values of β_{PF} at room temperature corresponding to all the measured samples are listed in Table II. PF field lowering coefficient is given by

$$\beta_{\text{PF}} = \sqrt{\left(\frac{e^3}{\pi \epsilon_0 k}\right)}, \quad (5)$$

where the optical frequency dielectric constant k should be used in this equation²⁹ ($k \sim n^2$, with n the refractive index of the dielectric material). Refractive index for HfO_2 ranges from 1.7 to 1.9,²⁹ so the theoretical dielectric constant of HfO_2 at optical frequencies is about 3.6. We have also included dielectric constant at optical frequencies obtained from our measurements in Table II. Although the good fit of PF plots, β_{PF} , is not constant for all the samples, values corresponding to Asd_2 (2.75) and Asd_3 (2.94) samples (Asd_1 sample has not been measured, but it is to be expected the same behavior) approach the theoretical HfO_2 value. Silicon nitride layer can be responsible for the lower values obtained compared to the theoretical value. However, when samples are submitted to RTA or when the silicon nitride thickness is the smallest (2.96 nm), dielectric constant does not agree with the theoretical value at all. It seems that when samples are submitted to RTA before high- k deposition, reactions between both dielectrics are promoted, so HfO_2 properties move away from its theoretical properties. If the silicon nitride layer is too thin, the interface with the substrate cannot completely keep its quality. When HfO_2 was deposited directly on $n\text{-Si}$ substrate, we have found that the dielectric constant at optical frequencies is about 0.43.⁸ In that case, a SiO_x layer is unintentionally obtained between

HfO₂ and silicon substrate. Silicon nitride barrier layer can prevent some reaction between hafnium oxide and substrate, at least, when no RTA is applied and its thickness is big enough.

IV. SUMMARY

The electrical characteristics of Al/HfO₂/SiN_x:H/*n*-Si MIS capacitors have been studied. HfO₂ was grown by HPS, while silicon nitride was grown by ECR-CVD. Samples with thicker silicon nitride dielectric layer show larger flatband voltage shift, which can be due to hydrogen accumulated in the film. DIGS density is also bigger in the thickest samples, as we have measured by conductance transients and by flatband voltage transients, but this can be due to our measurement range: If these defects are close to dielectric/semiconductor interface, they exchange charge with substrate fast enough not to be detected by our measurements. We have experimentally observed that DLTS provides overestimated values for very thin silicon nitride layers in the specific case of the HfO₂/SiN_x:H/Si system. That is due to the big amount of charge trapped at the hole well, which is formed in the valence band at the hafnium oxide–silicon nitride interface. Leakage current dependencies on voltage and temperature followed the PF conduction mechanism. The optical frequency dielectric constant only fits with the theoretical value in the case of the as-deposited films. When samples are submitted to RTA, some electrical characteristics changed: D_{it} does not vary significantly, but DIGS density is higher and the optical frequency dielectric constant does not fit with the theoretical value at all. From all of these measurements, it seems that if silicon nitride layer is not thick enough, reactions of the HfO₂ layer with silicon substrate cannot be avoided. Moreover, the RTA applied to the silicon nitride before the high-*k* growth seems to promote the reaction between both dielectrics, so slow state density inside the dielectric is bigger and dielectric constant measured does not fit with theoretical values. However, the electrical characteristics can be improved if we compare these results with those of Al/HfO₂/Si structures.

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